IN THE CLAIMS

1. (Currently amended) A semiconductor memory device comprising:

a memory cell array including word lines arranged in a row direction, bit lines and ~~a~~ column selecting lines arranged in a column direction, and memory cell array blocks arranged in the column direction;

internal voltage generating lines arranged between the memory cell array blocks;

a column decoder arranged on a first side of the memory cell array and configured to select one of the column selecting lines;

~~an~~ a first and a second internal voltage generating circuit arranged on ~~both~~ the first side and a second side, respectively, of the memory cell array, the first and second internal voltage generating circuits ~~and~~ configured to compare a reference voltage to an internal voltage and to generate a comparing signal, the comparing signal different from the internal voltage; and

drivers arranged on both ends of the internal voltage generating lines, respectively, and configured to supply the internal voltage to the internal voltage generating lines in response to the comparing signal.

2. (Previously presented) The device of claim 1, the drivers comprising:

first drivers coupled to the internal voltage generating lines on the first side of the memory cell array; and

second drivers coupled to the internal voltage generating lines on the second side of the memory cell array.

3. (Previously presented) The device of claim 2, further comprising:

a first external voltage applying pad configured to apply an external voltage to the first drivers; and

a second external voltage applying pad configured to apply the external voltage to the second drivers.

4. (Original) The device of claim 3, further comprising:

a first external voltage applying pin configured to apply the external voltage to the first external voltage applying pad; and

a second external voltage applying pin configured to apply the external voltage to the second external voltage applying pad.

5. (Previously presented) The device of claim 2, the column decoder comprising:

a column address input buffer for receiving and buffering the column address;

a column address pre-decoder for pre-decoding the buffered column address; and

column selecting line driving circuits for driving the column selecting lines in response to the pre-decoded column address, wherein the second drivers are arranged between the column selecting line driving circuits.

6. (Currently amended) A device comprising:

a memory cell array having a first and a second memory cell array block;

an internal voltage generating line arranged between the first and the second memory cell array blocks;

a first and a second active internal voltage generating circuit arranged on a first and second side, respectively, of the memory cell array, the first and second active internal voltage generating circuits configured to output a comparison signal that is generated by a comparator, the comparator configured to generate the comparison signal based upon the difference between a reference voltage and an internal voltage; and

a first and a second driver coupled to the first and the second active internal voltage generating circuits, respectively, and coupled to a first and a second end, respectively, of the internal voltage generating line, the first and second drivers configured to supply the internal voltage to the internal voltage generating line in response to the comparison signal.

7. (Original) The device of claim 6, further comprising:

a first external voltage pad configured to apply an external voltage to the first driver; and

a second external voltage pad configured to apply the external voltage to the second driver.

8. (Original) The device of claim 7, further comprising:

a first external voltage pin coupled to the first external voltage pad; and

a second external voltage pin coupled to the second external voltage pad, the second external voltage pin separated from the first external voltage pin.

9. (Currently amended) A ~~layout~~ method of fabricating a semiconductor memory device, the method comprising:

arranging ~~a plurality of~~ memory cell array blocks of a memory cell array in a column direction;

arranging ~~a plurality of~~ internal voltage generating lines between the ~~plurality of~~ memory cell array blocks;

arranging a column decoder adjacent to ~~one~~ a first side of the memory cell array;

arranging ~~an~~ a first active internal voltage generating circuit adjacent to ~~two sides~~ the first side of the memory cell array, the first active internal voltage generating circuit including a first comparator; ~~and~~

arranging a second active internal voltage generating circuit adjacent to a second side of the memory cell array, the second active internal voltage generating circuit including a second comparator;

arranging ~~a plurality of drivers of the active internal voltage generating circuit on two sides of the plurality of the internal voltage generating lines.~~ first driver adjacent to the first side of the memory cell array, an output of the first driver coupled to a first end of one of the internal voltage generating lines, an output of the first comparator coupled to an input of the first driver; and

arranging a second driver adjacent to the second side of the memory cell array, an output of the second driver coupled to a second end of the one of the internal voltage generating lines, an output of the second comparator coupled to an input of the second driver.

10. (Currently amended) The method of claim 9, wherein arranging the ~~drivers~~ first driver and arranging the second driver comprises:

~~arranging first drivers of the active internal voltage generating circuit on one side of the internal voltage generating lines;~~

~~arranging second drivers of the active internal voltage generating circuit on another side of the internal voltage generating lines; and~~

~~arranging~~ coupling a first external voltage ~~applying pad for applying an external voltage to the first drivers and a second external voltage applying pad for applying the external voltage to the second drivers.~~ pad to another input of the first driver, the first external voltage pad configured to be electrically connected to an external voltage;

coupling a second external voltage pad to another input of the second driver, the second external voltage pad configured to be electrically connected to the external voltage.

11. (Currently amended) The method of ~~claim 9~~, claim 10, further comprising:

coupling the first external voltage pad to a first external voltage pin; and

coupling the second external voltage pad to a second external voltage pin.

~~wherein a first external voltage applying pin for applying the external voltage to the first external voltage applying pad is separated from a second external voltage applying pin for applying the external voltage to the second external voltage applying pad.~~

12. (Currently amended) A method comprising:

directly coupling an output of a first comparator in a first active internal voltage circuit to an input of a first driver;

coupling [[a]]an output of the first driver ~~from a first active internal voltage circuit~~ to a first end of an internal voltage generating line that is structured to supply an internal voltage to a memory cell array block; ~~and~~

directly coupling an output of a second comparator in a second active internal voltage circuit to an input of a second driver; and

coupling [[a]]an output of the second driver ~~from a second active internal voltage circuit~~ to a second end of the internal voltage generating line.

13. (Original) The method of claim 12, further comprising:

simultaneously driving the internal voltage generating line with the first driver and the second driver.

14. (Original) The method of claim 12, further comprising:

supplying an external voltage to the first driver using a first external voltage pad; and

supplying the external voltage to the second driver using a second external voltage pad.

15. (Original) The method of claim 12, wherein coupling the first driver and coupling the second driver comprises:

arranging the first driver and the second driver between two column selecting lines.